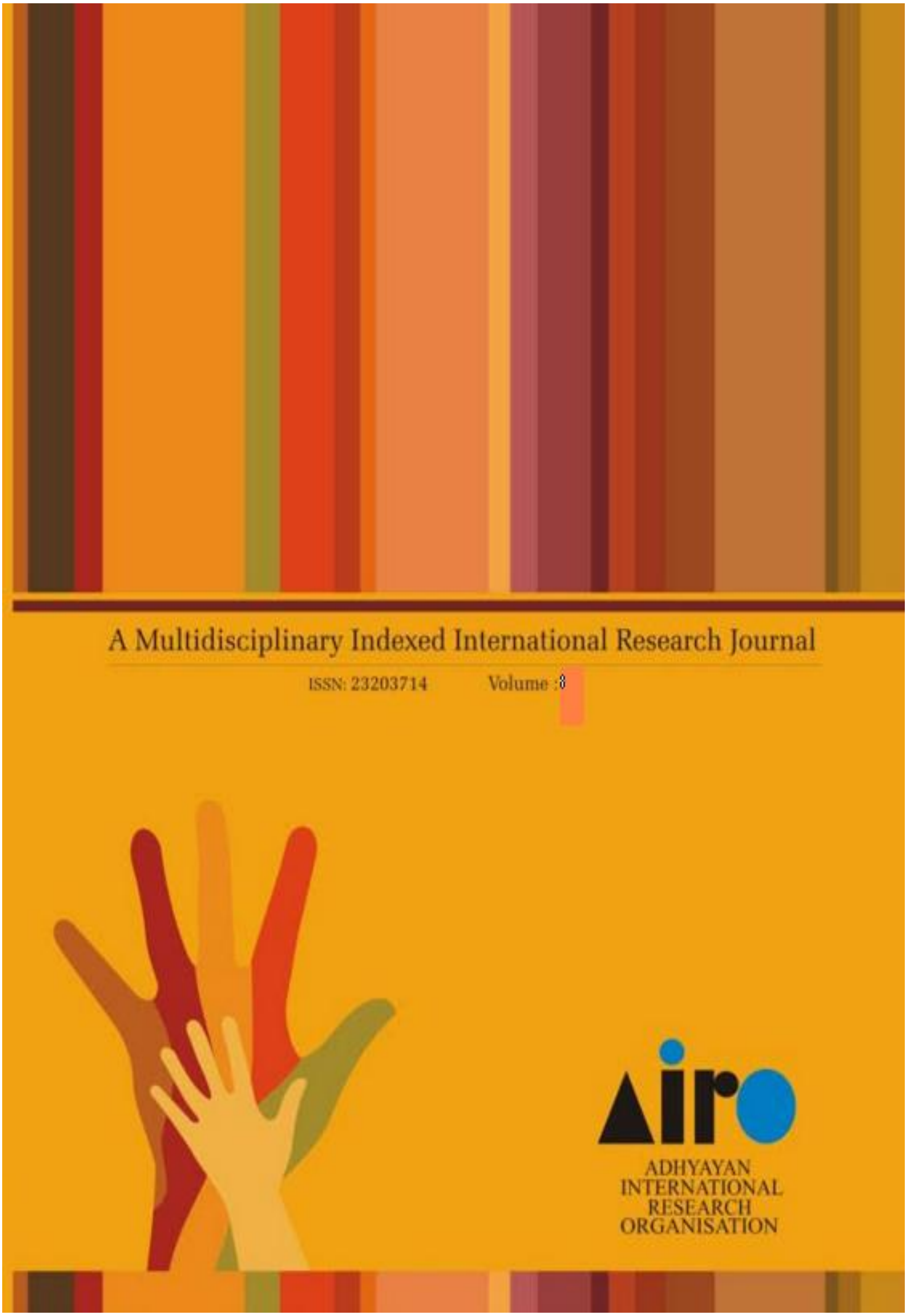
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IMPLEMENTATION OF SDR (SOFT WARE DEFINED RADIO) RECEIVER USING SIXPORT SUBSTRATE INTEGRATED WAVE GUIDE TECHNOLOGY

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ABSTRACT

With recent advances in semiconductor processing technology and the development of reconfigurable devices, high bit-rate software-defined radio (SDR) has become practical for commercial applications. This thesis proposes an SDR receiver platform based on a new substrate integrated waveguide six-port structure. This proposed SDR receiver platform operates from 22 to 26 GHz and it is designed to be robust, low cost, and suitable for different communication schemes. In this work , the receiver is demonstrated to support quadrature phase-shift keying and 16 quadrature amplitude modulation schemes. System-level simulation is made and prototype circuits are fabricated to evaluate the system performance. It is found that the combination of SDR and six-port technology can provide a great flexibility in system configuration, a significant reduction in system development cost, and also a high potential for software reuse. The proposed receiver shows a possible application of universal direct demodulator for future SDR terminals in various wireless communication systems.

Keywords—Digital receiver, six-port junction, 16 quadrature amplitude modulation (QAM16), software-defined radio (SDR), substrate integrated waveguide (SIW).

INTRODUCTION

Traditional radio communication systems need a lot of hardware components such as demodulator, detector, filter, etc. which makes the platform cost very high for undergraduate level study and research. But the Laboratory exercises and studies on that aspect are necessary for related teachers and students.

Software Defined Radio (SDR) makes it possible to implement the radio communication process simply with software. Comparing to the traditional radio communication systems, SDR omits all the hardware and replaces them by pure software. This solution also gives a great advantage in flexibility because a SDR receiver is able to decode all the signals.

THE NEED FOR SOFTWARE DEFINED RADIO

In the past few decades, the field of wireless communications has been developing and advancing at a rapid pace. Nearly all new electronic devices implement some sort of wireless communications, be it in the form of Wi-Fi, Bluetooth, or cellular technologies like CDMA or LTE. Each of these different radio systems has its own specific protocols. Consequently, these different radio systems had to be implemented using hardware configurations.

Hardware radios use physical components which are not easily modified. Consequently, this static nature gives hardware radios several limitations. First, needing different hardware setups for each radio technology can use significant amounts of space, especially if a particular setup needs several different radio technologies. Second, implementing separate hardware protocols becomes expensive to systems needing to use many different radio standards. Cellular phone technology provides a key example of this phenomenon. In cellular phone technology, entire nations and regions have attempted to standardize the radio protocol; however, cell phones still need to support old standards still in use and alternate standards in different regions so a single phone can operate in many locations.

ARCHITECTURE OF SOFTWARE DEFINED RADIO

All SDR systems retain some overarching, basic distinguishing characteristics. As the name suggests, software radios are known for their use of software, but all communication systems – either software or hardware – must have some sort of hardware front-end to send and received electric signals. In addition to this front-end hardware, all software radio systems have some sort of reprogrammable general purpose processor which handles the signal processing for the system. In is this general purpose processor that differentiates software radios from hardware radios. In a hardware-defined radio, the processing unit would not be easily changeable. All software radios possess both front-end hardware and a reprogrammable processing unit, but different SDR systems differ in implementation of this basic setup.

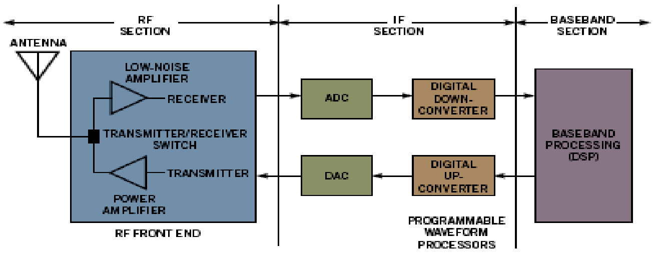

Fig 1. Architechture of SDR

As a modular design, SDRs are limited by the restrictions of their components. More precisely, SDRs cannot have better performance than its most limited component will allow. All stages in the SDR architecture shown in fig 1. Depend on the other stages, making it essential that a SDR system has no significant flaws. Unfortunately, one of the most limited parts of SDRs is the front end hardware. Consequently, the research and development of SDRs over the past decade has benefited from hardware improvements in addition to software improvements. Even so, a SDR designer must be aware of its potential hardware limitations and adjust the system accordingly. The front-end hardware designs of modern SDR receivers and transmitters can be broken down into two main categories: super heterodyne and homodyne.

SIX-PORT CIRCUIT DESIGN

As a key RF component of the proposed receiver, an SIW six-port circuit was designed for the proposed SDR receiver platform. The SIW technology, as a part of the substrate integrated circuits (SICs) family, has been proposed recently, as an attractive technology for low-loss, low-cost and high density integration of microwave and millimeter-wave components and subsystem.

Six-port technology has been under development for the past thirty years starting with microwave and millimeter-wave measurement applications; In principle, the six-port consists of linear circuits with dividers and combiners interconnected in such a way that four or "N" different vectorial additions of reference signal and signal to be measured (receiver signal) are obtained. The prototype of the SIW six-port circuit and six-port software receiver is shown in Fig 2 & Fig.3. The circuit is fabricated on a Rogers RT/Duroid 5880 laminates substrate with. It consists of two SIW power dividers, two SIW 90 3-dB hybrid couplers, and some in-line phase shifters. SIW-to-micro strip transitions are also integrated in the circuit. Unlike the other six-port junctions, for the direct receiver system, the proposed six-port structure is a true "six-port" without need for any external connecting terminals.

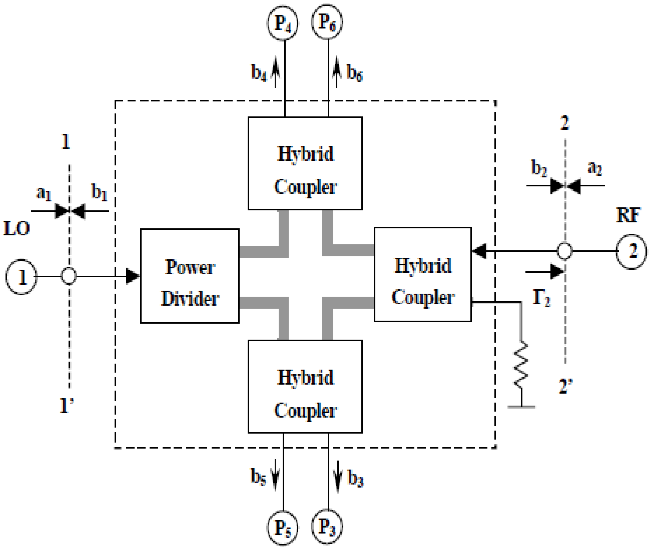

Fig 2: Six Port circuit

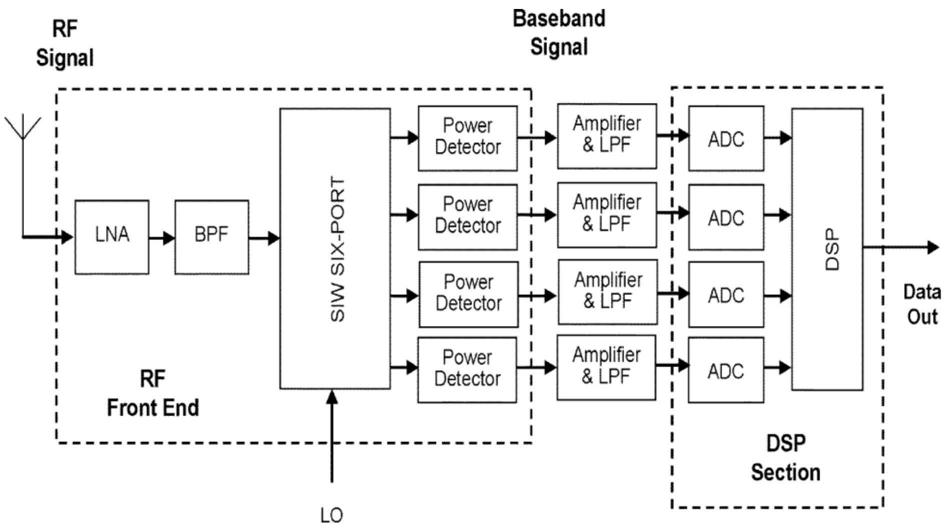

Fig 3: Architecture of six-port software receiver

Therefore, the structure is more compact at lower cost. The SIW six-port circuit is designed to operate over the frequency band of 22–26 GHz with the center frequency at 24 GHz. The scattering parameters of the proposed SIW six-port circuit are summarized for the center frequency at 24 GHz. The six-port junction is simulated using Agilent's High-Frequency Structure Simulator (HFSS) 5.6, the simulation model includes SIW power dividers, SIW couplers, SIW phase shifters, and SIW-to-micro strip transitions. All the SIW components are modeled using the equivalent rectangular waveguide with effective width. Considering the time efficiency of simulation, the K connectors are not included in the HFSS simulation model, while the measurement results naturally involve effects of the K connectors at each port. It can be found Fig 4. Flowchart of six-port receiver algorithm, that, at the center frequency, the reflection coefficients and are less than 21 dB and the isolation between the RF and LO ports is less than 21 dB. The transmission coefficients are lose to the theoretically predicted value (6 dB).

RECEIVER ALGORITHMS

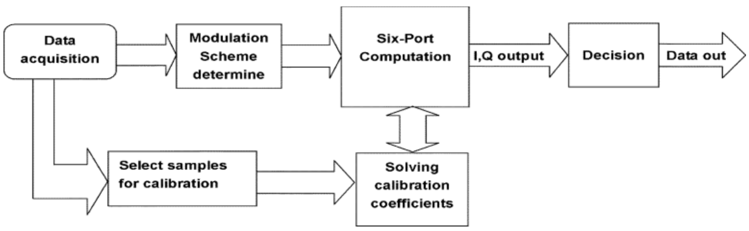

Fig:4 Flowchart of six-port receiver algorithm

The complex constants related to six-port circuit *Xi*, *Yi* that are obtained from calibration to arrive at required receiver demodulation. Table 1 and 2 show the simulated demodulation results for virtual six-port circuit for QPSK and QAM16 modulations when using suitable algorithms.For an SDR receiver platform, the DSP computation algorithms and calibration methods are crucial, shows the algorithm flowchart of the SDR six-port receiver. After the data acquired from the antenna, some samples are selected for calibration. After calibration, the six-port calibration coefficients can be generated, the coefficients are then used in six-port computation to calculate the in-phase and quadrature (I-Q) data. Following a decision algorithm, the signals are thus demodulated. This process is a universal demodulation algorithm for six-port receivers.

In the proposed receiver platform, a real-time six-port calibration method is adopted and the demodulation results for different modulation schemes are analyzed. For the six-port receiver, the ratio of amplitude, frequency, and phase between the LO signal (port 1) and RF signal (port 2) can be calculated from the power output at the other four ports with the complex constants known by calibration procedures. For a six-port receiver circuit, normally the leakage of the received signal to the LO reference port is small and may be neglected.

$$X_i=A_xp_1+A_{x2}p_2+A_{x3}p_3+C_x \quad \text{-------} (1)$$

$$Y_i=A_yp_1+A_{y2}p_2+Ay_3p_3+Cy \quad \text{-------} (2)$$

where X_i and Y_i are the calculated output data, where as A_{xj},A_{yj} (j=1,2,3) and are calibration parameters be determined. p_1 p_2 and p_3 are power ratios at the output detectors of the six-port.

Table 1 Demodulation data result for QPSK signal

Input	Output	Input	Output
1 ∠45°	1.0205∠ 46.66°	1 ∠225°	1.0000∠ 224.68°
1∠ 135°	0.9595∠ 139.42°	1 ∠315°	1.0365∠ 315.45°

Table 2 Demodulation data result for QAM16 signal

Input	Output	Input	Output
4.2426 ∠45°	4.1636 ∠47.46°	1.4142∠ 225°	1.5123∠ 227.20°
3.1623∠ 18.43°	3.1548 ∠18.90°	3.1623∠ 251.56°	3.1305∠ 249.71°
1.4142∠ 45°	1.2892 ∠43.18°	4.2426 ∠225°	4.2693∠ 224.02°
3.1623 ∠71.56°	2.9562 ∠43.15°	3.1623∠ 198.43°	3.1952 ∠201.29°
3.1623∠341.57°	3.2395∠341.25°	3.1623∠ 108.44°	2.9198 ∠111.52°
4.2426 ∠315°	4.3099 ∠341.82°	1.4142∠ 145°	1.2758∠ 143.24°
3.1623∠ 288.44°	3.1222 ∠287.17°	3.1426 ∠161.57°	3.0527 ∠166.60°
1.4142∠ 315°	1.4511∠ 311.64°	4.2426 ∠145°	3.9331∠ 141.67°

The simulated demodulation results show that the receiver has an accuracy of ±5 degrees in

phase and ±0.4 dB in amplitude. It is found that actual six-port circuits do indeed comply with

above resolution in phase and amplitude.

BASIC BLOCKS OF MATLAB

The basic building block of MATLAB is MATRIX. The fundamental data type is the array. Vectors, scalars, real matrices and complex matrix are handled as specific class of this basic data type. The built in functions are optimized for vector operations. No dimension statements are required for vectors or arrays.

MATLAB FILES

MATLAB has three types of files for storing information. They are: M-files and MAT-files.

RESULTS AND ANALYSIS

Within the operating frequency band of the receiver (1 GHz), two modulation schemes (i.e., QPSK, QAM16) are selected to test performances of the proposed SDR receiver. System-level simulation is made using HP-ADS and MATLAB-Simulink, and the bit error rate (BER) measurement results of the proposed receiver platform are also presented. The simulated input and output amplitudes and phases of QPSK signals are given in Figure 2. The INPUT is pseudorandom bit sequence QPSK signals at the input of the vector modulator. The OUTPUT is the same bit sequence, which is demodulated after six-port computation and decision. It can be seen the input signals and output signals are exactly the same, which confirms the operating principle of the proposed SDR receiver.

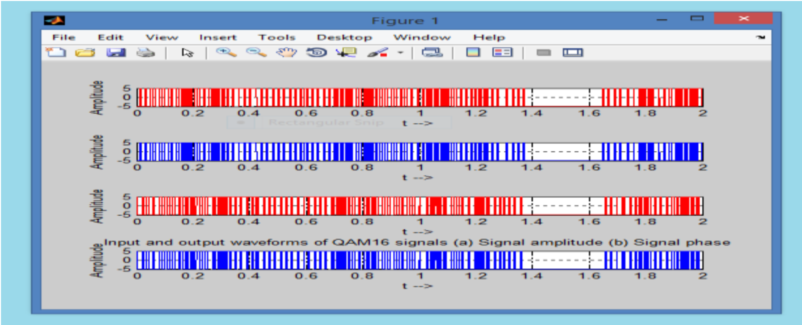

Fig 2: Input and output waveforms of QPSK signals

(a)Signal amplitu (b) Signal phase.

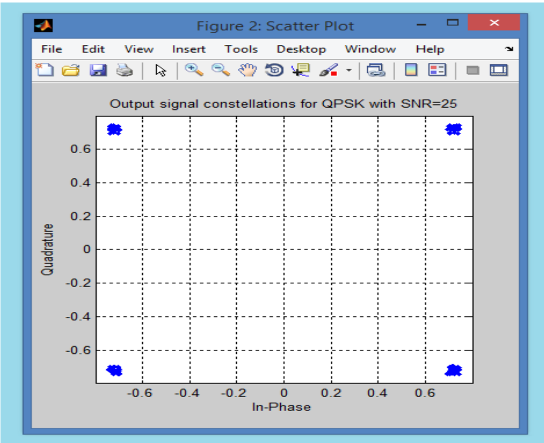

Fig: 3(a)

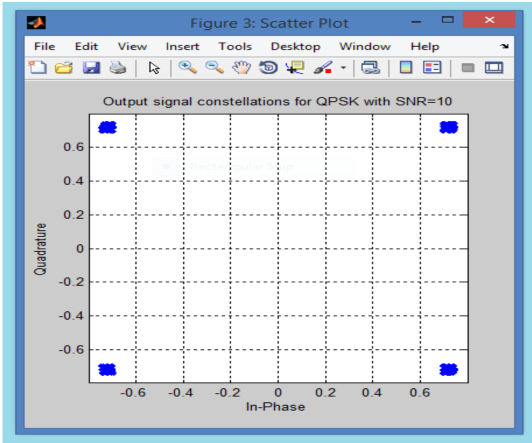

Fig: 3(b)

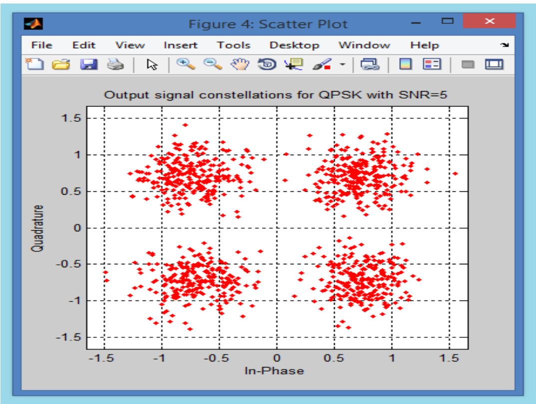

Fig: 3(c)

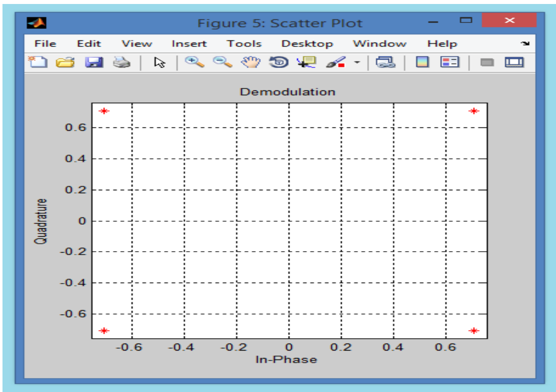

Fig: 3(d)

Fig 3: Simulated output signal constellations for QPSK with different SNR

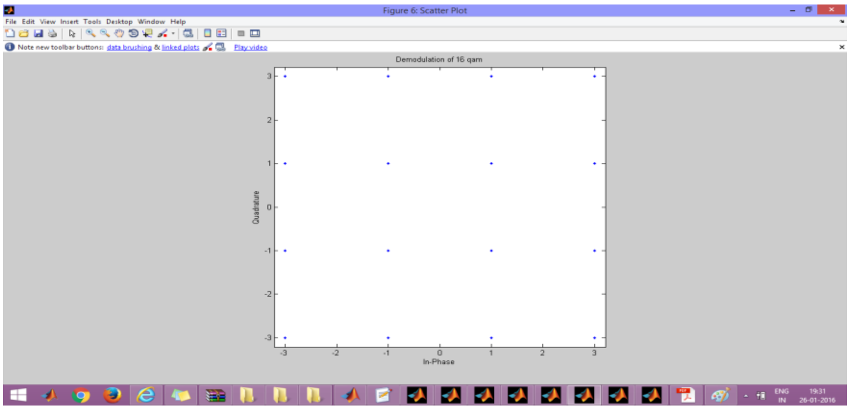

Fig: 4 Demodulated QAM 16 Signal

The signals are digitalized by four AD9433 ADC integrated in two FPGA boards. The receiver algorithms are implemented in the two FPGA processors. The BER analyzer receives the demodulated signal from DSP board1 and evaluates the BER values of the receiver system. An additional white noise generator Agilent N8975A is used for the adjacent signal interference or noise measurements. Figure shows a photograph of our test setup. It consists of one RF signal generator, one vector signal modulator, one dc power supply, one 3-dB power divider and two RF up-converters, an SIW six-port with RF power detectors, one baseband amplifier evaluation module board, and two FPGA development boards. Simulated and measured BER versus for the two modulation schemes are presented in Figure where is the average energy of a modulated bit and is the noise power spectral density. The QPSK and QAM16 signals are generated from a vector modulator without coding. The simulated BER results are obtained from MATLAB-Simulink with carrier RF frequency from 22 to 26 GHz, considering the same conditions of power inputs and interferences. The measured BER curve is obtained at the center frequency (1 GHz) of the receiver platform.

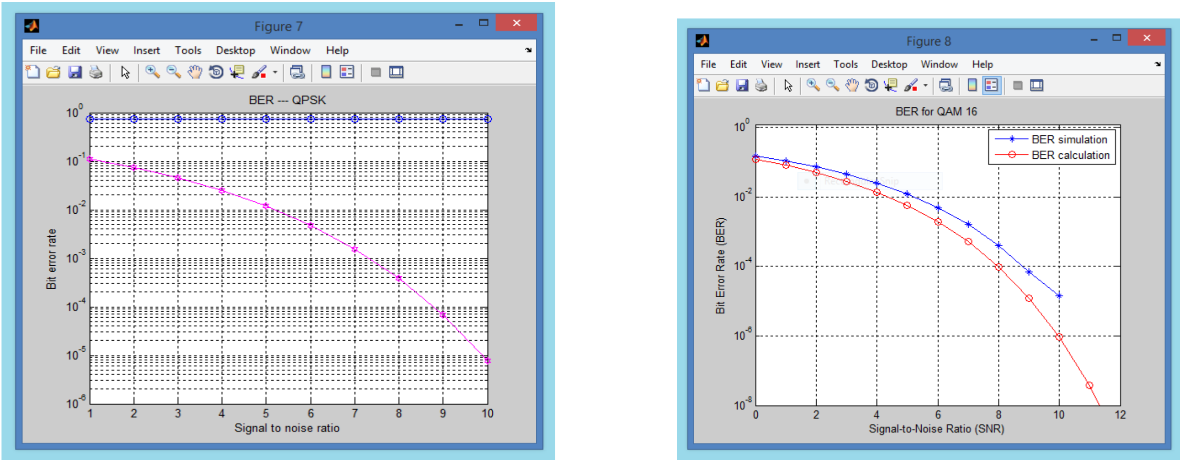

Figure 5: BER Measurement for QPSK and QAM16

It can be seen that the simulated and measured BER curves are in excellent agreement. It is observed that the receiver BER is less than for higher than 10.5 dB (QPSK) and 15 dB (QAM16).

CONCLUSION

This thesis has presented recent results obtained on the analysis of SDR technology in a direct six-port receiver designed for multimode RF and millimeter-wave communications. A six-port SDR receiver platform has been analyzed and implemented. This platform adopts a new SIW six-port structure at the RF front-end, which realizes wideband direct down conversion for low-cost and mass-producible SDR applications. Based on the six-port front-end, the demodulation algorithms have been designed and the demodulation results and BER performance of the SDR receiver for two different modulation schemes (QPSK, QAM16) have been described. The simulation and measurement results are very encouraging, showing a possible universal receiver solution for future software-defined radio applications in various wireless communication systems. Our current effort is to implement orthogonal frequency division multiplexing (OFDM) demodulation in this SDR receiver platform.

FUTURE SCOPE

While some consumer-based SDR systems currently exist, most are not easy enough to use for the average consumer. Therefore, the future of SDR adoption lies in making them robust and easy to use for non-technical users. Then, many developers are working to make simple, cheap, and small software radios that can be easily modified and used by consumers.

This is not the ultimate goal of software radio systems; however, as researchers hope SDRs can provide advanced functionality impossible in classical hardware radios.

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